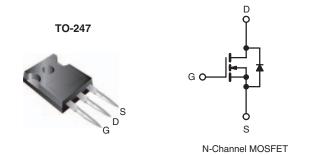


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	50	500				
$R_{DS(on)}\left(\Omega\right)$	V _{GS} = 10 V	0.40				
Q _g (Max.) (nC)	150					
Q _{gs} (nC)	20					
Q _{gd} (nC)	80					
Configuration	Single					



FEATURES

- · Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- · Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP450PbF
Leau (FD)-liee	SiHFP450-E3
SnPb	IRFP450
SIFD	SiHFP450

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	500	V	
Gate-Source Voltage			V_{GS}	± 20		
Continuous Drain Current	V _{GS} at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1-	14	А	
	V _{GS} at 10 V	T _C = 100 °C	ID	8.7		
Pulsed Drain Current ^a			I _{DM}	56		
Linear Derating Factor				1.5	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	760	mJ	
Repetitive Avalanche Current ^a			I _{AR}	8.7	Α	
Repetitive Avalanche Energy ^a			E _{AR}	19	mJ	
Maximum Power Dissipation	T _C = 25 °C		P_{D}	190	W	
Peak Diode Recovery dV/dt ^c			dV/dt	3.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	00	
Soldering Recommendations (Peak Temperature)	for '	10 s		300 ^d	°C	
Mounting Torque	6.22.04.1	0.00 140		10	lbf ⋅ in	
	6-32 or M3 screw			1.1	N · m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 7.0 mH, R_G = 25 Ω , I_{AS} = 14 A (see fig. 12).
- c. $I_{SD} \le 14$ A, $dI/dt \le 130$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRFP450, SiHFP450

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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	40		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.65		

SPECIFICATIONS T _J = 25 °C,	unless other	vise noted					
PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static						•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	o 25 °C, I _D = 1 mA	-	0.63	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		2.0	-	4.0	٧
Gate-Source Leakage	I _{GSS}	V _G	V _{GS} = ± 20 V		-	± 100	nA
Zone Oata Walkana Busin Oursel	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$		00 V, V _{GS} = 0 V	-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V	_{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.4 A ^b	-	-	0.40	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 5	0 V, I _D = 8.4 A ^b	9.3	-	-	S
Dynamic				I.	•	•	
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0 MHz, see fig. 5		-	2600	-	pF
Output Capacitance	C _{oss}			-	720	-	
Reverse Transfer Capacitance	C _{rss}			-	340	-	
Total Gate Charge	Qg		I _D = 14 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	150	nC
Gate-Source Charge	Q_{gs}	V _{GS} = 10 V		-	-	20	
Gate-Drain Charge	Q _{gd}			-	-	80	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 250 V, I_D = 14 A, R_G = 6.2 Ω , R_D = 17 Ω , see fig. 10 ^b		-	17	-	ns
Rise Time	t _r			-	47	-	
Turn-Off Delay Time	t _{d(off)}			-	92	-	
Fall Time	t _f			-	44	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	- nH
Internal Source Inductance	L _S			-	13	-	
Drain-Source Body Diode Characteristic	s			I.			
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	56	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 14 A, V _{GS} = 0 V ^b		-	-	1.4	V
Body Diode Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = 14 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s}^b$		-	540	810	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	4.8	7.2	μС
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and I				L _D)	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

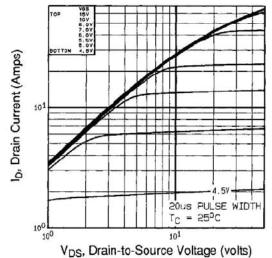


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

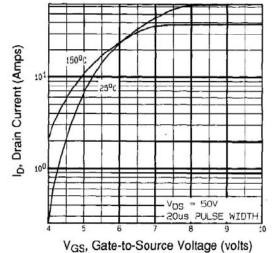


Fig. 3 - Typical Transfer Characteristics

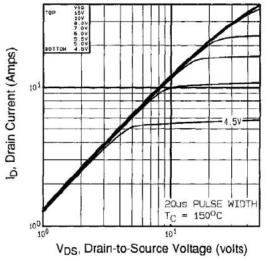


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

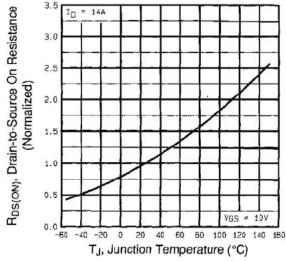


Fig. 4 - Normalized On-Resistance vs. Temperature

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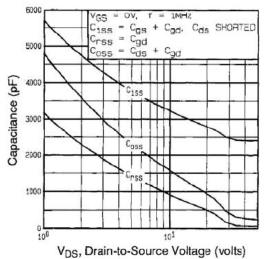


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

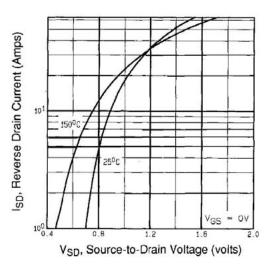


Fig. 7 - Typical Source-Drain Diode Forward Voltage

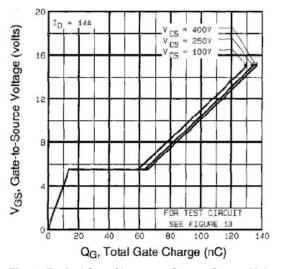


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

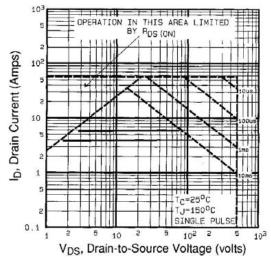


Fig. 8 - Maximum Safe Operating Area





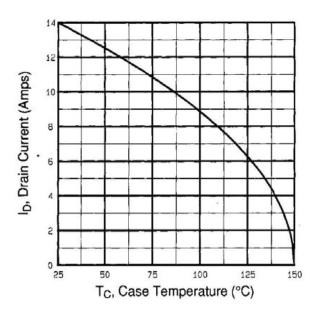


Fig. 9 - Maximum Drain Current vs. Case Temperature

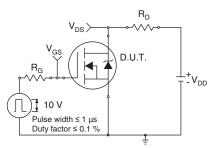


Fig. 10a - Switching Time Test Circuit

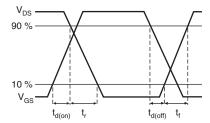


Fig. 10b - Switching Time Waveforms

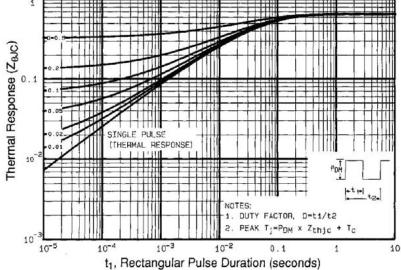


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

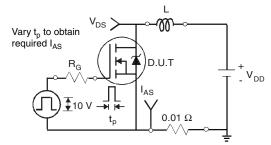


Fig. 12a - Unclamped Inductive Test Circuit

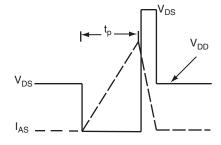


Fig. 12b - Unclamped Inductive Waveforms

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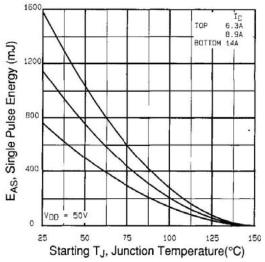


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

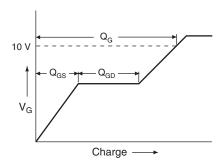


Fig. 13a - Basic Gate Charge Waveform

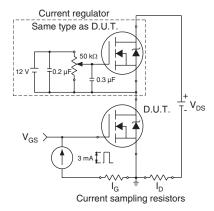
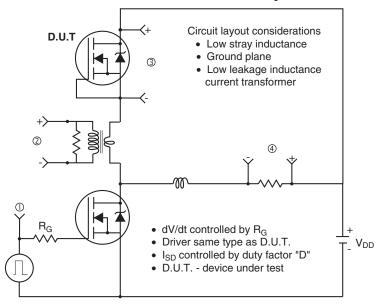


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



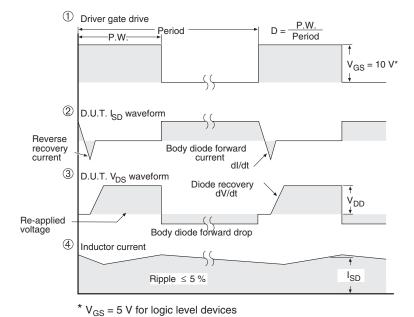


Fig. 14 - For N-Channel

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